ANALOG DEVICES

Triple 8-Bit, 140 MSPS A/D Converter

AD9483

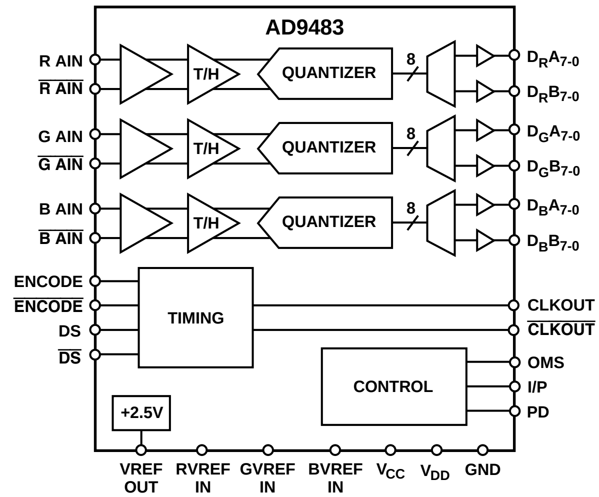
FEATURES

- 140 MSPS Guaranteed Conversion Rate
- 100 MSPS Low Cost Version Available
- 330 MHz Analog Bandwidth
- 1 V p-p Analog Input Range
- Internal +2.5 V Reference
- Differential or Single-Ended Clock Input
- 3.3 V/5.0 V Three-State CMOS Outputs
- Single or Demultiplexed Output Ports
- Data Clock Output Provided
- Low Power: 1.0 W Typical
- +5 V Converter Power Supply

APPLICATIONS

- RGB Graphics Processing
- High Resolution Video
- LCD Monitors and Projectors
- Micromirror Projectors
- Plasma Display Panels
- Scan Converters

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9483 is a triple 8-bit monolithic analog-to-digital converter optimized for digitizing RGB graphics signals from personal computers and workstations. Its 140 MSPS encode rate capability and full-power analog bandwidth of 330 MHz supports display resolutions of up to 1280 × 1024 at 75 Hz with sufficient input bandwidth to accurately acquire and digitize each pixel.

To minimize system cost and power dissipation, the AD9483 includes an internal +2.5 V reference and track-and-hold circuit. The user provides only a +5 V power supply and an encode clock. No external reference or driver components are required for many applications. The digital outputs are three-state CMOS outputs. Separate output power supply pins support interfacing with 3.3 V or 5 V logic.

The AD9483's encode input interfaces directly to TTL, CMOS, or positive-ECL logic and will operate with single-ended or differential inputs. The user may select dual channel or single channel digital outputs. The Dual Channel (demultiplexed) mode interleaves ADC data through two 8-bit channels at one-half the clock rate. Operation in Dual Channel mode reduces the speed and cost of external digital interfaces while allowing the ADCs to be clocked to the full 140 MSPS conversion rate. In the Single Channel mode, all data is piped at the full clock rate to the Channel A outputs and the ADCs conversion rate is limited to 100 MSPS. A data clock output is provided at the Channel A output data rate for both Dual-Channel or Single-Channel output modes.

Fabricated in an advanced BiCMOS process, the AD9483 is provided in a space-saving 100-lead MQFP surface mount plastic package (S-100) and is specified over the 0°C to +85°C temperature range.

REV. A

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AD9483–SPECIFICATIONS (V_{CC} = +5 V, V_{DD} = +3.3 V, external reference, ENCODE = maximum conversion rate differential PECL)

Parameter	Temperature	Test Level	AD9483KS-140			AD9483KS-100			Units
			Min	Typ	Max	Min	Typ	Max	
RESOLUTION				8			8		Bits
DC ACCURACY									
Differential Nonlinearity	+25°C	I		0.8	1.25/–1.0		0.8	1.25/–1.0	LSB
	Full	VI			1.50/–1.0			1.50/–1.0	LSB
Integral Nonlinearity	+25°C	I		0.9	1.50/–1.50		0.9	1.50/–1.50	LSB
	Full	VI			1.75/–1.75			1.75/–1.75	LSB
No Missing Codes	Full	VI		Guaranteed			Guaranteed		
Gain Error[1]	+25°C	I		±1	±2		±1	±2	% FS
Gain Tempco[1]	Full	V		160			160		ppm/°C
ANALOG INPUT									
Input Voltage Range (With Respect to $\overline{AIN}$)	Full	V		±512			±512		mV p–p
Compliance Range AIN or $\overline{AIN}$	Full	V	1.8		3.2	1.8		3.2	V
Input Offset Voltage	+25°C	I		±4	±16		±4	±16	mV
	Full	VI			±20			±20	mV
Input Resistance	+25°C	I	35	83		35	83		kΩ
	Full	VI	25			25			kΩ
Input Capacitance	+25°C	V		4			4		pF
Input Bias Current	+25°C	I		17	36		17	36	µA
	Full	VI			50			50	µA
Analog Bandwidth, Full Power	+25°C	V		330			330		MHz
REFERENCE OUTPUT									
Output Voltage	Full	VI	+2.4	+2.5	+2.6	+2.4	+2.5	+2.6	V
Temperature Coefficient	Full	V		110			110		ppm/°C
SWITCHING PERFORMANCE									
Maximum Conversion Rate	Full	VI	140			100			MSPS
Minimum Conversion Rate	Full	IV			10			10	MSPS
Encode Pulsewidth High (t_{EH})	+25°C	IV	2.8		50	4.0		50	ns
Encode Pulsewidth Low (t_{EL})	+25°C	IV	2.8		50	4.0		50	ns
Aperture Delay (t_A)	+25°C	V		1.5			1.5		ns
Aperture Delay Matching	+25°C	V		100			100		ps
Aperture Uncertainty (Jitter)	+25°C	V		2.3			2.3		ps rms
Data Sync Setup Time (t_{SDS})	+25°C	IV	0			0			ns
Data Sync Hold Time (t_{HDS})	+25°C	IV	0.5			0.5			ns
Data Sync Pulsewidth (t_{PWDS})	+25°C	IV	2.0			2.0			ns
Output Valid Time (t_V)[2]	Full	VI	4.0	6.3		4.0	6.3		ns
Output Propagation Delay (t_{PD})[2]	Full	VI		8.0	10		8.0	10	ns
Clock Valid Time (t_{CV})[3]	Full	VI	3.8	6.2		3.8	6.2		ns
Clock Propagation Delay (t_{CPD})[3]	Full	VI		8.0	10		8.0	10	ns
Data to Clock Skew (t_V–t_{CV})	Full	VI	–1.0	0	1.0	–1.0	0	1.0	ns
Data to Clock Skew (t_{PD}–t_{CPD})	Full	VI	–2.0	0	2.0	–2.0	0	2.0	ns
DIGITAL INPUTS									
Input Capacitance	+25°C	V		3			3		pF
DIFFERENTIAL INPUTS									
Differential Signal Amplitude (V_{ID})	Full	IV	400			400			mV
HIGH Input Voltage (V_{IHD})	Full	IV	0.4		V_{CC}	0.4		V_{CC}	V
LOW Input Voltage (V_{ILD})	Full	IV	0			0			V
Common-Mode Input (V_{ICM})	Full	IV	1.5			1.5			V
HIGH Level Current (I_{IH})	Full	VI			1.2			1.2	mA
LOW Level Current (I_{IL})	Full	VI			1.2			1.2	mA
VREF IN									
Input Resistance	+25°C	V		2.5			2.5		kΩ

Parameter	Temperature	Test Level	AD9483KS-140 Min	Typ	Max	AD9483KS-100 Min	Typ	Max	Units
SINGLE-ENDED INPUTS									
HIGH Input Voltage (V_{IH})	Full	IV	2.0		V_{CC}	2.0		V_{CC}	V
LOW Input Voltage (V_{IL})	Full	IV	0		0.8	0		0.8	V
HIGH Level Current (I_{IH})	Full	VI			1			1	mA
LOW Level Current (I_{IL})	Full	VI			1			1	mA
DIGITAL OUTPUTS									
Logic "1" Voltage	Full	VI	V_{DD} – 0.05			V_{DD} – 0.05			V
Logic "0" Voltage	Full	VI			0.05			0.05	V
Output Coding				Binary			Binary		
POWER SUPPLY									
V_{CC} Supply Current	Full	VI			215			215	mA
V_{DD} Supply Current	Full	VI			60			60	mA
Total Power Dissipation[4]	Full	VI		1.0	1.3		1.0	1.3	W
Power-Down Supply Current	+25°C	V		4	20		4	20	mA
Power-Down Dissipation	+25°C	V		20	100		20	100	mW
DYNAMIC PERFORMANCE[5]									
Transient Response	+25°C	V		1.5			1.5		ns
Overvoltage Recovery Time	+25°C	V		1.5			1.5		ns
Signal-to-Noise Ratio (SNR) (Without Harmonics)									
f_{IN} = 19.7 MHz	+25°C	V		45			45		dB
f_{IN} = 49.7 MHz	+25°C	I	41	44		41	44		dB
f_{IN} = 69.7 MHz	+25°C	V		44			44		dB
Signal-to-Noise Ratio (SINAD) (With Harmonics)									
f_{IN} = 19.7 MHz	+25°C	V		44			44		dB
f_{IN} = 49.7 MHz	+25°C	I	40	43		40	43		dB
f_{IN} = 69.7 MHz	+25°C	V		42			42		dB
Effective Number of Bits									
f_{IN} = 19.7 MHz	+25°C	V		7.0			7.0		Bits
f_{IN} = 49.7 MHz	+25°C	I	6.4	6.8		6.4	6.8		Bits
f_{IN} = 69.7 MHz	+25°C	V		6.8			6.8		Bits
2nd Harmonic Distortion									
f_{IN} = 19.7 MHz	+25°C	V		63			63		dBc
f_{IN} = 49.7 MHz	+25°C	I	50	58		50	58		dBc
f_{IN} = 69.7 MHz	+25°C	V		51			51		dBc
3rd Harmonic Distortion									
f_{IN} = 19.7 MHz	+25°C	V		56			56		dBc
f_{IN} = 49.7 MHz	+25°C	I	46	54		46	54		dBc
f_{IN} = 69.7 MHz	+25°C	V		51			51		dBc
Crosstalk	Full	V		55			55		dB

NOTES

[1]Gain error and gain temperature coefficient are based on the ADC only (with a fixed +2.5 V external reference).

[2]t_V and t_{PDF} are measured from the threshold crossing of the ENCODE input to valid TTL levels at the digital outputs. The output ac load during test is 5 pF.

[3]t_{CV} and t_{CPD} are measured from the threshold crossing of the ENCODE input to valid TTL levels at the digital outputs. The output ac load during test is 20 pF.

[4]Measured under the following conditions: analog input is –1 dBFS at 19.7 MHz.

[5]SNR/harmonics based on an analog input voltage of –1.0 dBFS referenced to a 1.024 V full-scale input range.

Typical thermal impedance for the S-100 (MQFP) 100-lead package: θ_{JC} = 10°C/W, θ_{CA} = 17°C/W, θ_{JA} = 27°C/W.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{CC}	+6 V
V_{DD}	+6 V
Analog Inputs	V_{CC} to 0.0 V
VREF IN, VREF OUT	V_{CC} to 0.0 V
Digital Inputs	V_{CC} to 0.0 V
Digital Output Current	20 mA
Operating Temperature	0°C to +85°C
Storage Temperature	–65°C to +150°C
Maximum Junction Temperature	+175°C
Maximum Case Temperature	+150°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C and sample tested at specified temperatures.

III – Periodically sample tested.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – 100% production tested at +25°C; guaranteed by design and characterization testing.

Table I. Output Coding

Step	AIN–$\overline{AIN}$	Code	Binary
255	≥0.512 V	255	1111 1111
254	0.508 V	254	1111 1110
253	0.504 V	253	1111 1101
•	•	•	•
•	•	•	•
•	•	•	•
129	0.006 V	129	1000 0001
128	0.002 V	128	1000 0000
127	–0.002 V	127	0111 1111
126	–0.006 V	126	0111 1110
•	•	•	•
•	•	•	•
•	•	•	•
2	–0.504 V	2	0000 0010
1	–0.508 V	1	0000 0001
0	≤–0.512 V	0	0000 0000

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9483KS-100	0°C to +85°C	Plastic Thin Quad Flatpack	S-100B
AD9483KS-140	0°C to +85°C	Plastic Thin Quad Flatpack	S-100B
AD9483/PCB	+25°C	Evaluation Board	

CAUTION

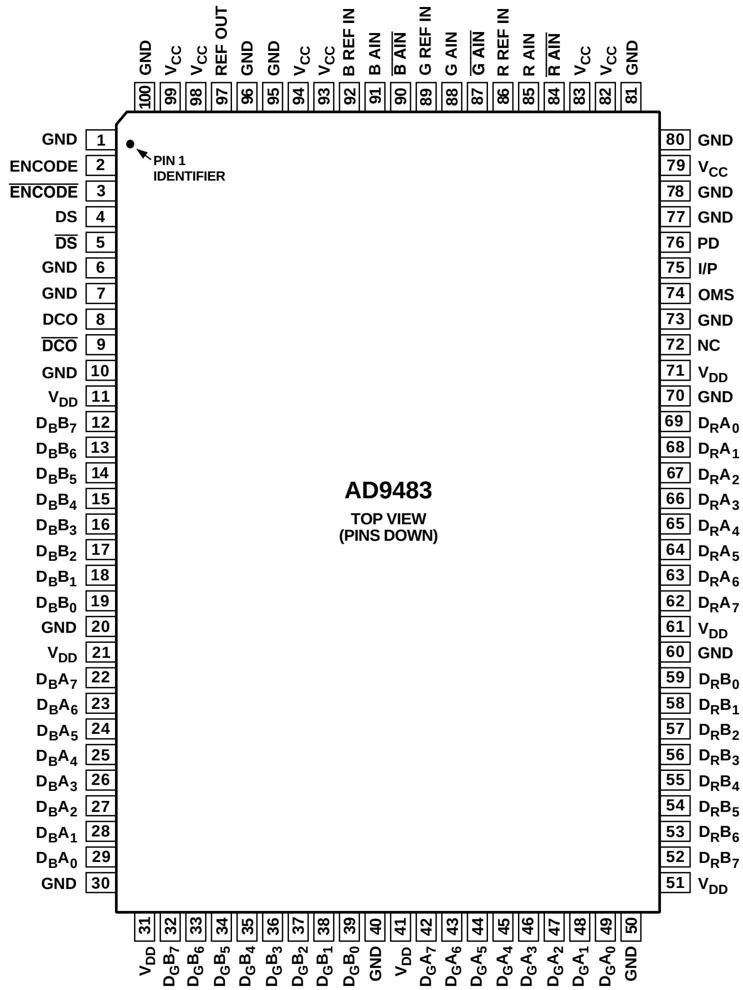
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9483 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN FUNCTION DESCRIPTIONS

Pin Number	Name	Function
1, 6, 7, 10, 20, 30, 40, 50, 60, 70, 73, 77, 78, 80, 81, 95, 96, 100	GND	Ground
2	ENCODE	Encode clock for ADC (ADC samples on rising edge of ENCODE).
3	$\overline{\text{ENCODE}}$	Encode clock complement (ADC samples on falling edge of $\overline{\text{ENCODE}}$).
4	DS	Data Sync Aligns output channels in Dual-Channel mode.
5	$\overline{\text{DS}}$	Data Sync complement.
8	DCO	Data Clock Output. Clock output at Channel A data rate.
9	$\overline{\text{DCO}}$	Data Clock Output complement.
11, 21, 31, 41, 51, 61, 71	V_{DD}	Output Power Supply. Nominally 3.3 V.
79, 82, 83, 93, 94, 98, 99	V_{CC}	Converter Power Supply. Nominally 5.0 V.
12–19	D_BB_7–D_BB_0	Digital Outputs of Converter “B,” Channel B. D_BB_7 is the MSB.
22–29	D_BA_7–D_BA_0	Digital Outputs of Converter “B,” Channel A. D_BA_7 is the MSB.
32–39	D_GB_7–D_GB_0	Digital Outputs of Converter “G,” Channel B. D_GB_7 is the MSB.
42–49	D_GA_7–D_GA_0	Digital Outputs of Converter “G,” Channel A. D_GA_7 is the MSB.
52–59	D_RB_7–D_RB_0	Digital Outputs of Converter “R,” Channel B. D_RB_7 is the MSB.
62–69	D_RA_7–D_RA_0	Digital Outputs of Converter “R,” Channel A. D_RA_7 is the MSB.
72	NC	No Connect.
74	OMS	Selects Single Channel or Dual Channel output mode, (HIGH = single, LOW = demuxed).
75	I/P	Selects interleaved or parallel output mode, (HIGH = interleaved, LOW = parallel).
76	PD	Power-Down and Three-State Select (HIGH = power-down).
84	$\overline{\text{R AIN}}$	Analog Input Complement for Converter “R.”
85	R AIN	Analog Input True for Converter “R.”
86	R REF IN	Reference Input for Converter “R” (+2.5 V Typical, ±10%).
87	$\overline{\text{G AIN}}$	Analog Input Complement for Converter “G.”
88	G AIN	Analog Input True for Converter “G.”
89	G REF IN	Reference Input for Converter “G” (+2.5 V Typical, ±10%).
90	$\overline{\text{B AIN}}$	Analog Input Complement for Converter “B.”
91	B AIN	Analog Input True for Converter “B.”
92	B REF IN	Reference Input for Converter “B” (+2.5 V Typical, ±10%).
97	REF OUT	Internal Reference Output (+2.5 V Typical); Bypass with 0.01 µF to Ground.

PIN CONFIGURATION
Plastic Thin Quad Flatpack (S-100B)



NC = NO CONNECT

TIMING

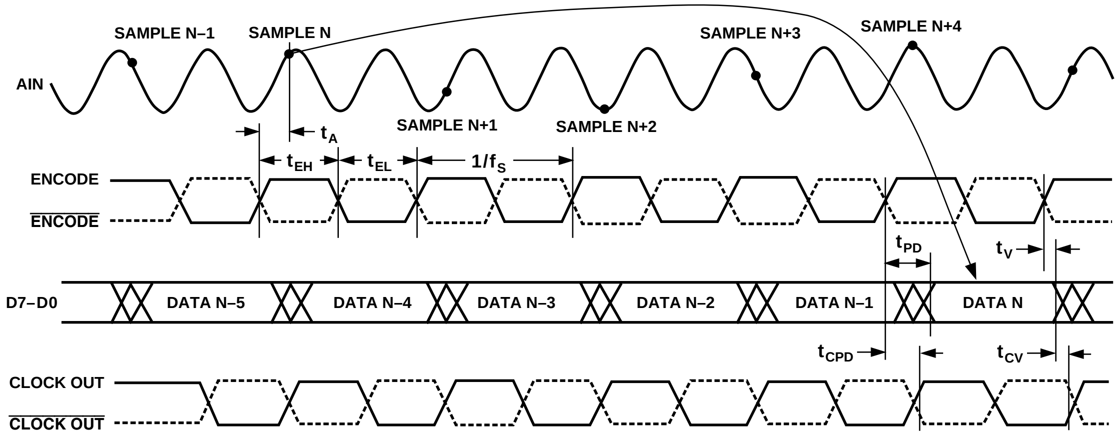


Figure 1. Timing—Single Channel Mode

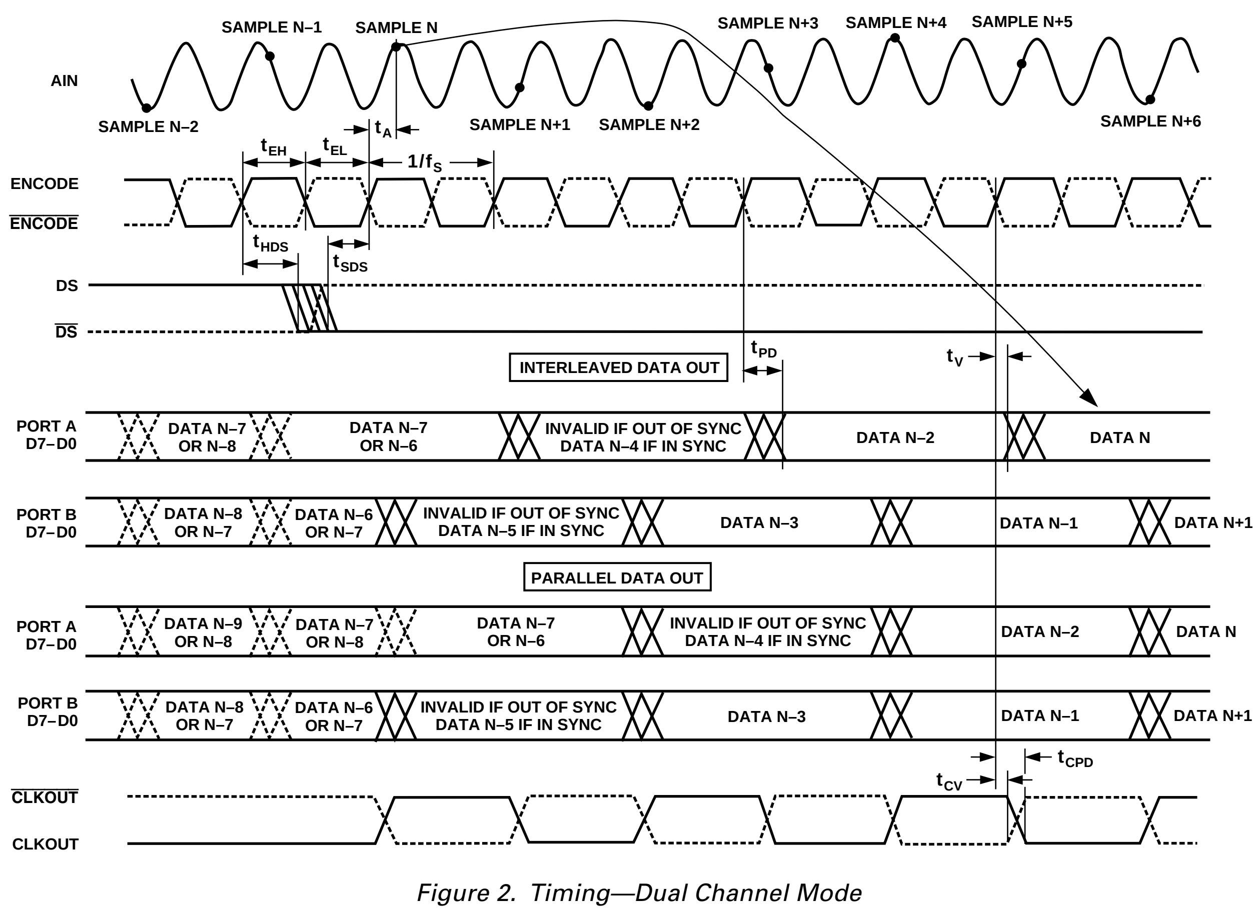


Figure 2. Timing—Dual Channel Mode

EQUIVALENT CIRCUITS

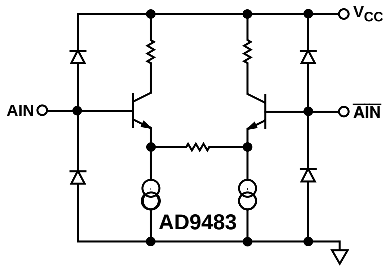


Figure 3. Equivalent Analog Input Circuit

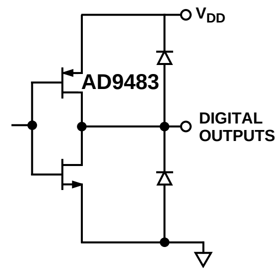


Figure 7. Equivalent Digital Output Circuit

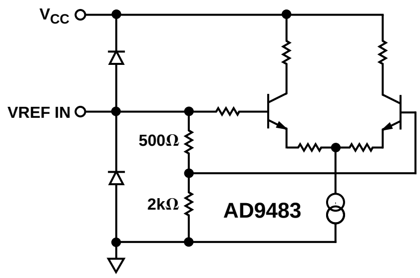


Figure 4. Equivalent Reference Input Circuit

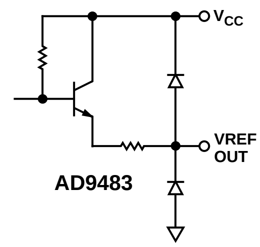


Figure 8. Equivalent Reference Output Circuit

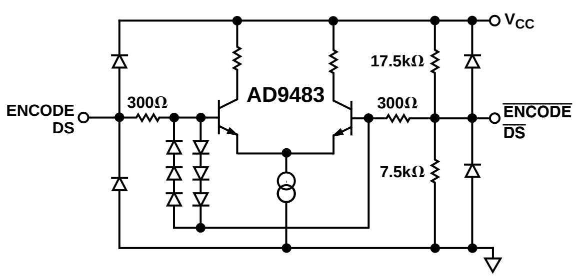


Figure 5. Equivalent Encode and Data Select Input Circuit

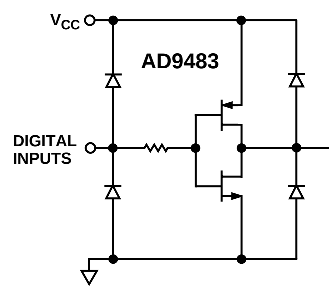


Figure 9. Equivalent Digital Input Circuit

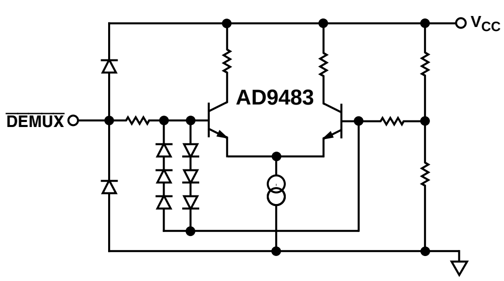


Figure 6. Equivalent $\overline{\text{DEMUX}}$ Input Circuit

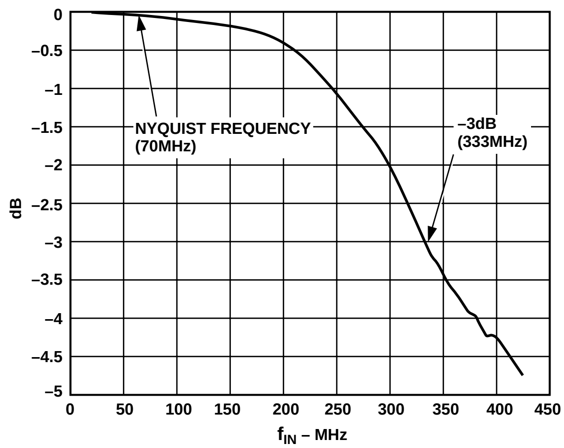


Figure 10. Frequency Response: f_S = 140 MSPS

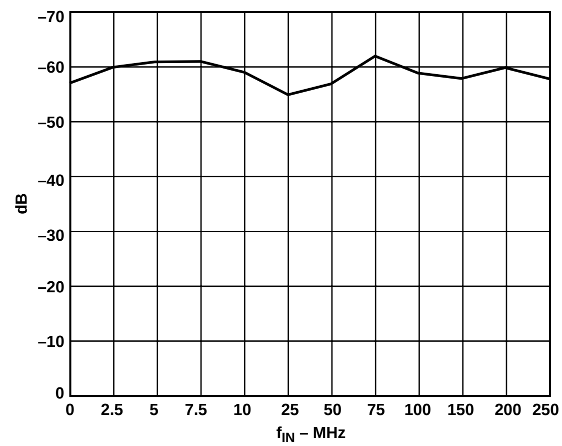


Figure 11. Crosstalk vs. f_{IN}: f_S = 140 MSPS

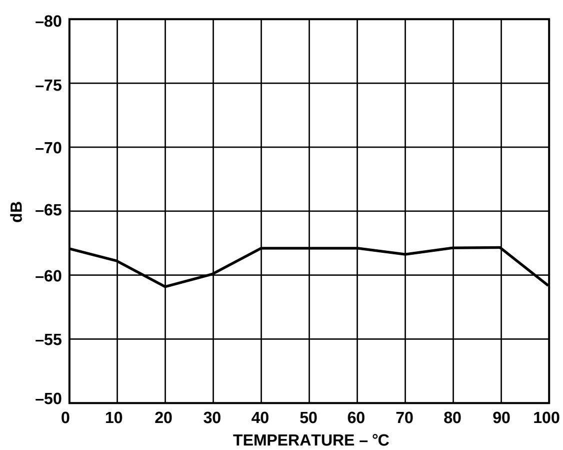


Figure 12. Crosstalk vs. Temperature: f_{IN} = 70 MHz

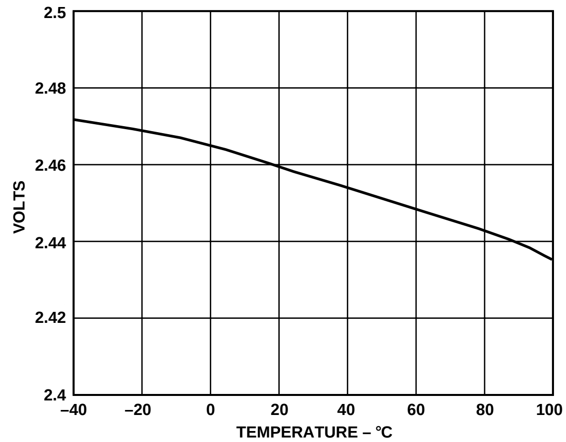


Figure 13. Reference Voltage vs. Temperature

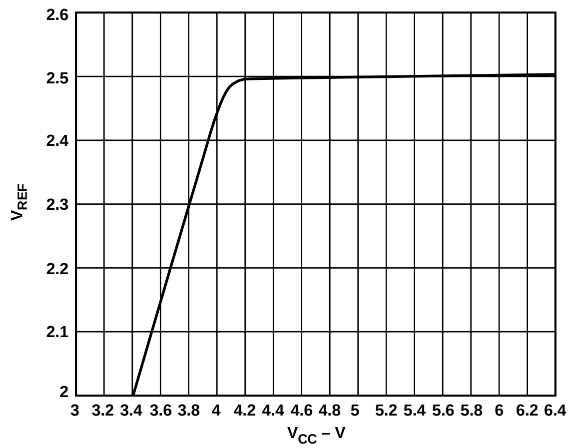


Figure 14. Reference Voltage vs. Power Supply Voltage

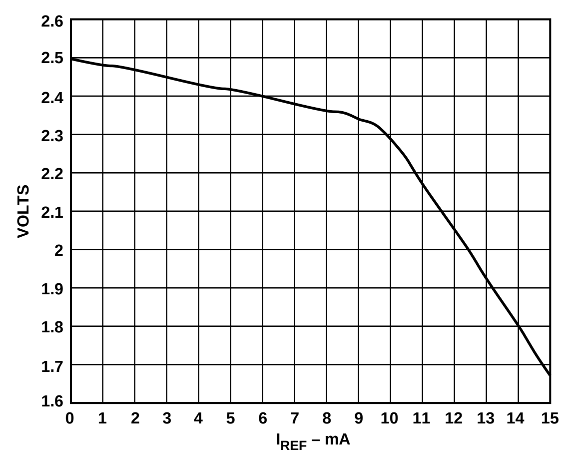


Figure 15. Reference Voltage vs. Reference Load

AD9483–Typical Performance Characteristics

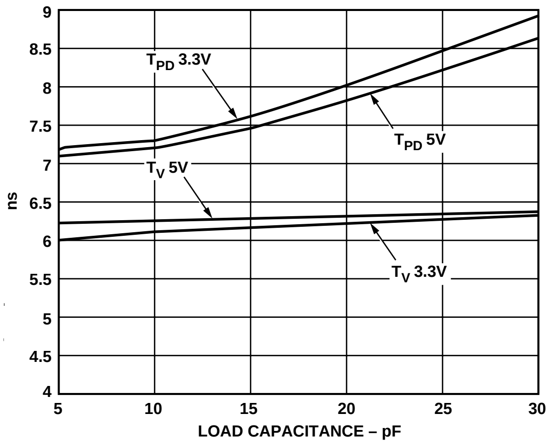


Figure 16. Clock Output Delay vs. Capacitance

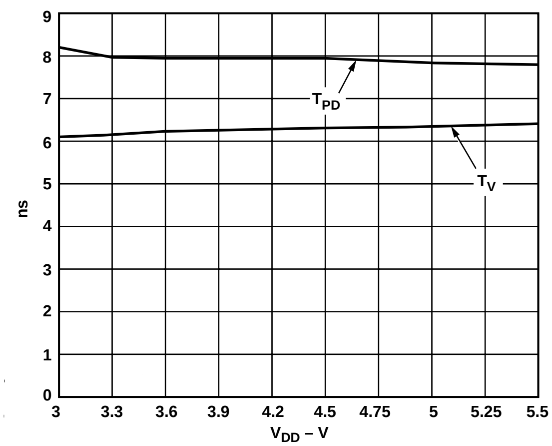


Figure 17. Output Delay vs. V_{DD}

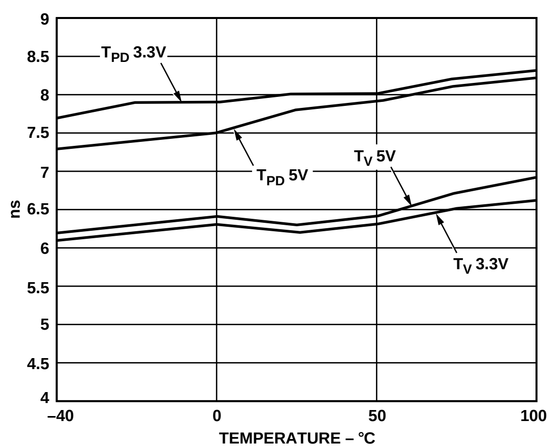


Figure 18. Output Delay vs Temperature

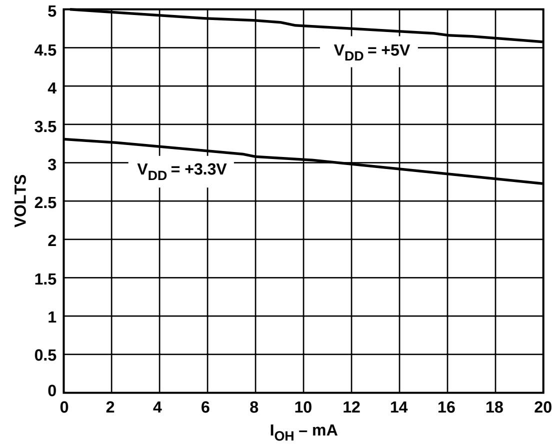


Figure 19. Output Voltage HIGH vs. Output Current

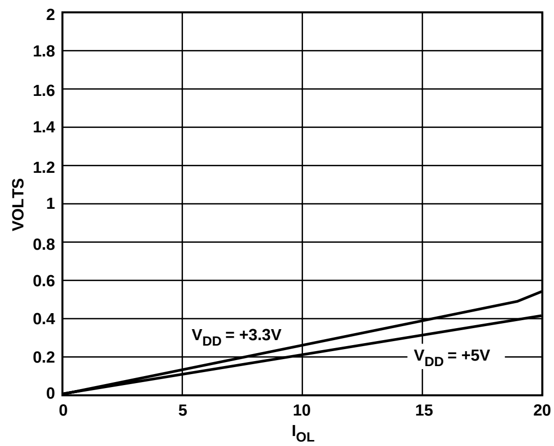


Figure 20. Output Voltage LOW vs. Output Current

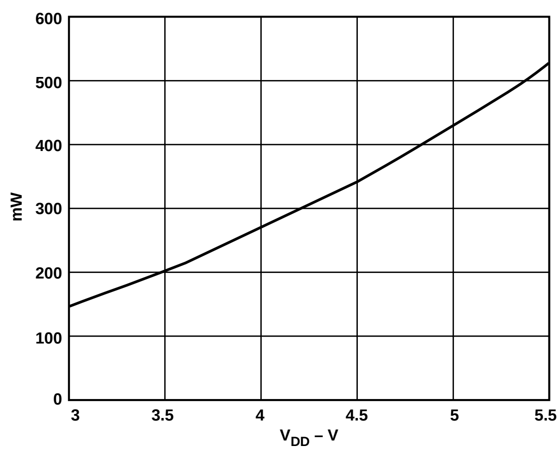


Figure 21. Output Power vs. V_{DD}, C_{LOAD} = 10 pF

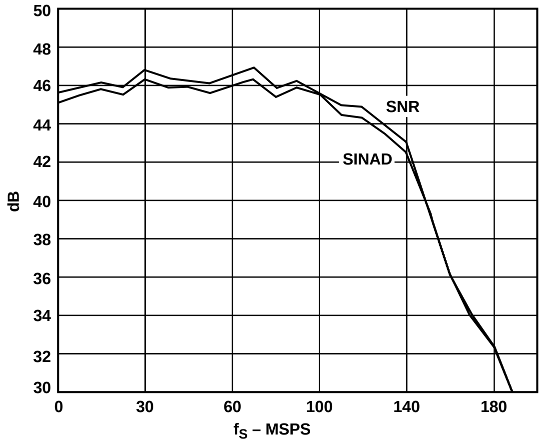


Figure 22. SNR vs. f_S: f_{IN} = 19.7 MHz

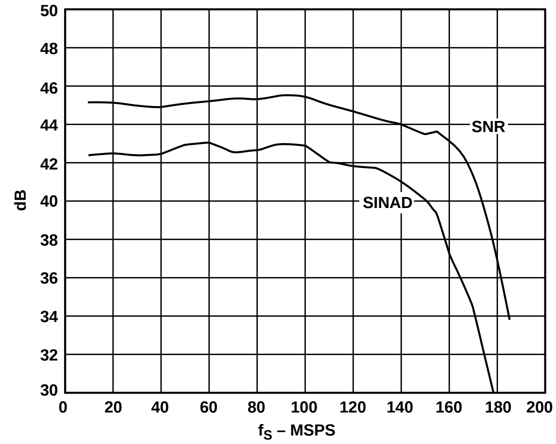


Figure 25. SNR vs f_S: f_{IN} = 71.7 MHz

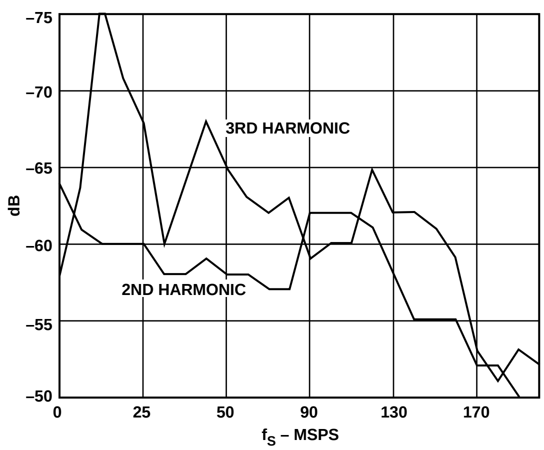


Figure 23. Harmonic Distortion vs. f_S: f_{IN} = 19.7 MHz

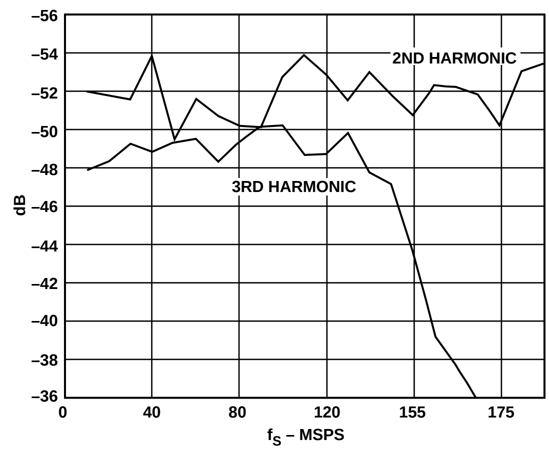


Figure 26. Harmonic Distortion vs f_S: f_{IN} = 71.7 MHz

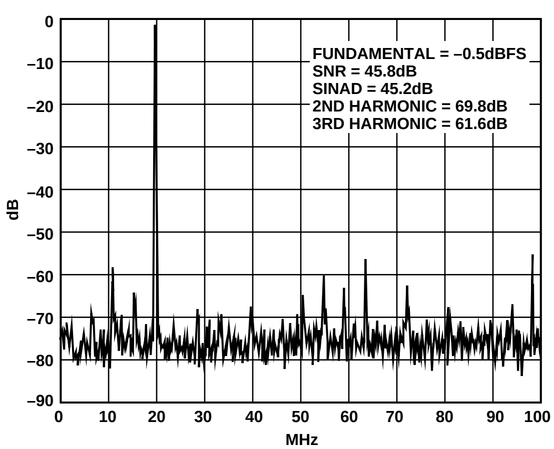


Figure 24. Spectrum: f_S = 140 MSPS, f_{IN} = 19.57 MHz

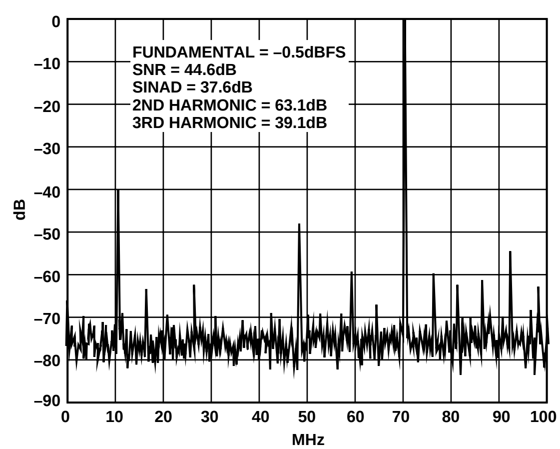


Figure 27. Spectrum: f_S = 140 MSPS, f_{IN} = 70.3 MHz

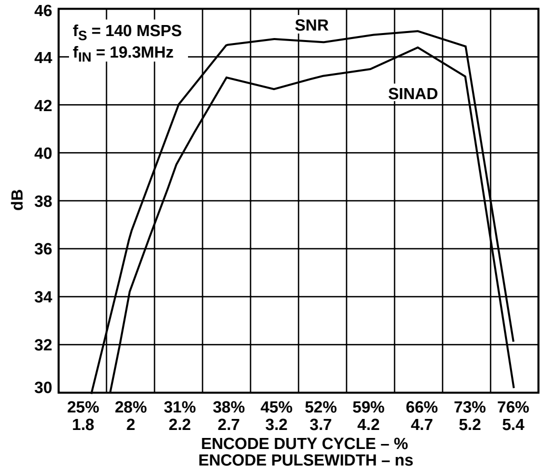


Figure 28. SNR vs. Clock Pulsewidth (t_{PWH}): f_S = 140 MSPS

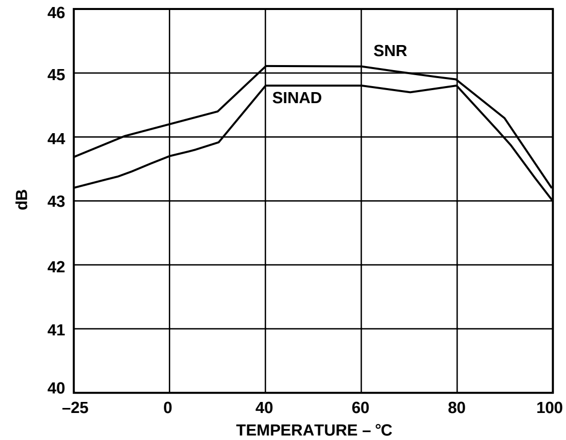


Figure 31. SNR vs. Temperature, f_S = 140 MSPS

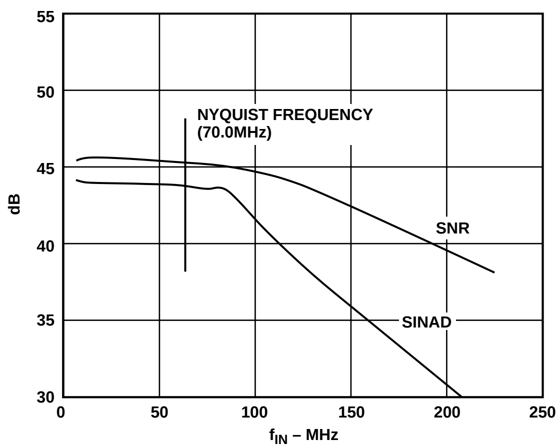


Figure 29. SNR vs. f_{IN}: f_S = 140 MSPS

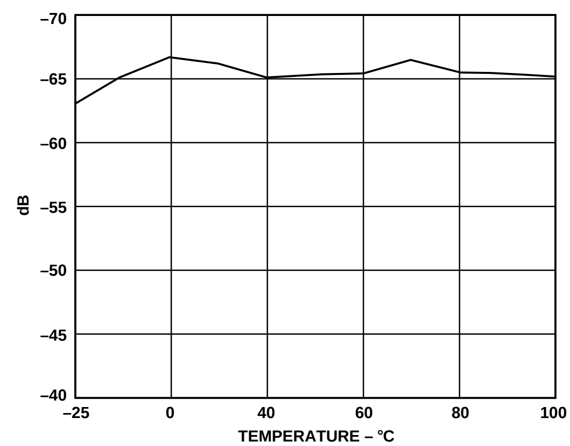


Figure 32. 2nd Harmonic vs. Temperature, f_S = 140 MSPS

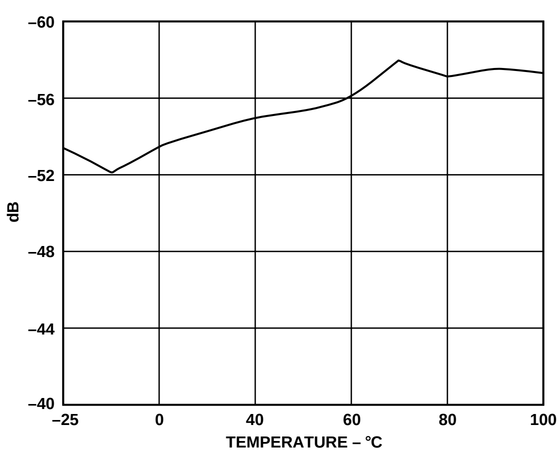


Figure 30. 3rd Harmonic vs. Temperature, f_S = 140 MSPS

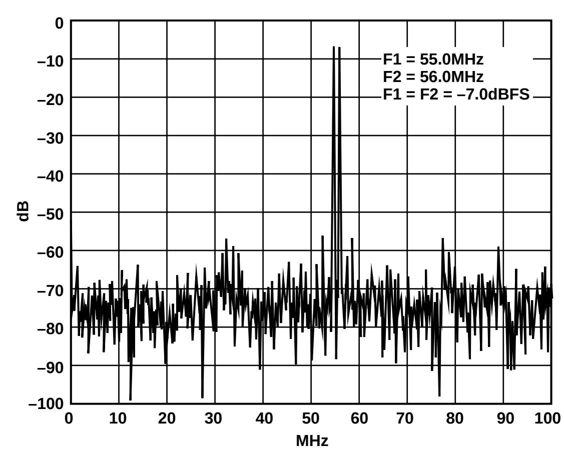


Figure 33. Two Tone Intermodulation Distortion

APPLICATION NOTES

Theory of Operation

The AD9483 combines Analog Devices' patented MagAmp bit-per-stage architecture with flash converter technology to create a high performance, low power ADC. For ease of use the part includes an on board reference and input logic that accepts TTL, CMOS or PECL levels.

Each of the three analog input signals is buffered by a high speed differential amplifier and applied to a track-and-hold (T/H) circuit. This T/H captures the value of the input at the sampling instant and maintains it for the duration of the conversion. The sampling and conversion process is initiated by a rising edge on the ENCODE input. Once the signal is captured by the T/H, the four Most Significant Bits (MSBs) are sequentially encoded by the MagAmp string. The residue signal is then encoded by a flash comparator string to generate the four Least Significant Bits (LSBs). The comparator outputs are decoded and combined into the 8-bit result.

If the user has selected Single Channel mode (OMS = HIGH) the 8-bit data word is directed to an A output bank. Data are strobed to the output on the rising edge of the ENCODE input with four pipeline delays. If the user has selected Dual Channel mode (OMS = LOW) the data are alternately directed between the A and B output banks and the data has five pipeline delays. At power-up, the N sample data can appear at either the A or B Port. To align the data in a known state, the user must strobe DATA SYNC (DS, $\overline{DS}$) per the conditions described in the Timing section.

Graphics Applications

The high bandwidth and low power of the AD9483 makes it very attractive for applications that require the digitization of presampled waveforms, wherein the input signal rapidly slews from one level to another, then is relatively stable for a period of time. Examples of these include digitizing the output of computer graphic display systems, and very high speed solid state imagers.

These applications require the converter to process inputs with frequency components well in excess of the sampling rate (often with subnanosecond rise times), after which the A/D must settle and sample the input in well under one pixel time. The architecture of the AD9483 is vastly superior to older flash architectures, which not only exhibit excessive input capacitance (which is very hard to drive), but can make major errors when fed a very rapidly slewing signal. The AD9483's extremely wide bandwidth Track/Hold circuit processes these signals without difficulty.

Using the AD9483

Good high speed design practices must be followed when using the AD9483. Decoupling capacitors should be physically as close as possible to the chip to obtain maximum benefit. We recommend placing a 0.1 µF capacitor at each power ground pin pair (14 total) for high frequency decoupling and including one 10 µF capacitor for local low frequency decoupling. Each of the three VREF IN pins should also be decoupled by a 0.1 µF capacitor.

The part should be located on a solid ground plane and output trace lengths should be short (<1 inch) to minimize transmission line effects. This will avoid the need for termination resistors on the output bus and reduces the load capacitance that needs to be driven, which in turn minimizes on-chip noise due to heavy current flow in the outputs. We have obtained optimum performance on our evaluation board by tying all V_{CC} pins to a quiet analog power supply system and tying all GND pins to a quiet analog system ground.

Minimum Encode Rate

The minimum sampling rate for the AD9483 is 10 MHz for the 140 MSPS and 100 MSPS versions. To achieve this sampling rate, the Track/Hold circuit employs a very small hold capacitor. When operated below the minimum guaranteed sampling rate, the T/H droop becomes excessive. This is first observed as an increase in offset voltage, followed by degraded linearity at even lower frequencies.

Lower effective sampling rates may be easily supported by operating the converter in Dual Port output mode and using only one output channel. A majority of the power dissipated by the AD9483 is static (not related to conversion rate), so the penalty for clocking at twice the desired rate is not high.

Digital Inputs

SNR performance is directly related to the sampling clock stability in A/D converters, particularly for high input frequencies and wide bandwidths.

ENCODE and Data Select (DS) can be driven differentially or single-ended. For single-ended operation, the complement inputs ($\overline{ENCODE}$, $\overline{DS}$) are internally biased to $V_{DD}/3$ (~1.5 V) by a high impedance on-chip resistor divider (Figure 5), but they may be externally driven to establish an alternate threshold if desired. A 0.1 µF decoupling capacitor to ground is sufficient to maintain a threshold appropriate for TTL or CMOS logic.

When driven differentially, ENCODE and DS will accommodate differential signals centered between 1.5 V and 4.5 V with a total differential swing ≥800 mV (V_{ID} ≥400 mV).

Note the 6-diode clock input protection circuitry in Figure 5. This limits the differential input voltage to ±2.1 V. When the diodes turn on, current is limited by the 300 Ω series resistor. Exceeding 2.1 V across the differential inputs will have no impact on the performance of the converter, but be aware of the clock signal distortion that may be produced by the nonlinear impedance at the converter.

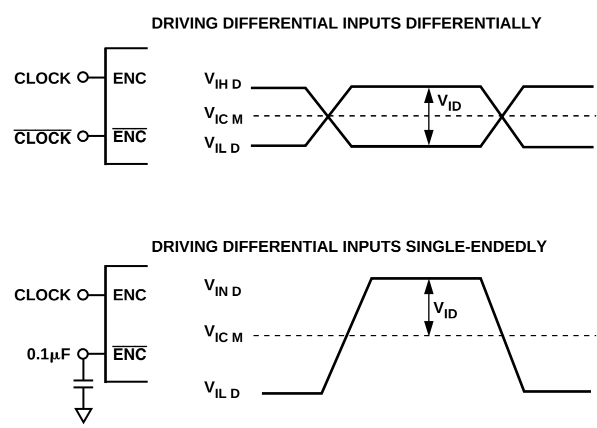


Figure 34. Input Signal Level Definitions

ADC Gain Control

Each of the three ADC channels has independent limited gain control. The full-scale signal amplitude for a given ADC is set by the dc voltage on its VREF In pin. The equation relating the full scale amplitude to VREF In is as follows: FS = (0.4) × (VREF IN). The three ADCs are optimized for a full-scale signal amplitude of 1 V, but will accommodate up to ±10% variation.

ADC Offset Control

The offset for each of the three ADCs can be independently controlled. For a single-ended analog input where the analog input is connected to a reference, offset can be adjusted simply by adjusting the dc voltage of the reference. For differential analog inputs, the user must provide the offset in their signal. Offset can be adjusted up or down as far as the common-mode input range will allow.

Power Dissipation

Power dissipation for the AD9483 has two components, V_{CC} and V_{DD}. Power dissipation from V_{CC} is relatively constant for a given supply voltage, whereas power dissipation from V_{DD} can vary greatly. V_{CC} supplies power to the analog circuity. V_{DD} supplies power to the digital outputs and can be approximated by the following equation:

$$P\,(V_{DD}) = 1/2\ C \times V^2 \times F \times N$$

C = Output Load Capacitance
V = V_{DD} Supply Voltage
F = Encode Frequency
N = Number of Outputs Switching

Nominally, C = 10 pF, V = 3.3 V, F = 140 MSPS, and N = 26. N comes from the 24 output bits plus two clock outputs, $P(V_{DD})$ = 197 mW.

Power-Down

The power-down function allows users to reduce power dissipation when output data is not required. A TTL/CMOS HIGH signal on pin 76, (PD), shuts down most of the chip and brings the total power dissipation to less than 100 mW. The internal bandgap voltage reference remains active during power-down mode to minimize reactivation time. If the power-down function is not desired, the PD pin should be tied to ground or held to a TTL/CMOS LOW level.

Bandgap Voltage Reference

The AD9483 internal reference, VREF OUT (Pin 97), provides a simple, cost effective reference for many applications. It exhibits reasonable accuracy and excellent stability over power supply and temperature variations. The reference output can be used to set the three ADCs' gain and offset. The reference is capable of providing up to 1 mA of additional current beyond the requirements of the AD9483.

As the ADC gain and offset are set by the reference inputs, some applications may require a reference with greater accuracy or temperature performance. In these cases, an external reference may be connected directly to the VREF IN pins. VREF OUT, if unused, should be left floating. Note, each of the three VREF IN pins will require up to 1 mA of current.

Modes of Operation

The AD9483 has three modes of operation, Single Channel output mode, and a Dual Channel output mode with two possible data formats, interleaved or parallel. Two pins control which mode of operation the chip is in, Pin 74 Output Mode Select (OMS) and Pin 75 Interleaved/Parallel Select (I/P). Table II shows the configuration required for each mode.

Table II. Output Mode Selection

MODE	OMS	I/P
Dual Channel—Parallel	LOW	LOW
Dual Channel—Interleaved	LOW	HIGH
Single Channel	HIGH	DON'T CARE

Demuxed Output Mode

In demuxed mode, (Pin 74 OMS = LOW), the ADC output data are alternated between the two output ports (Port A and Port B). This limits the data output rate to 1/2 the rate of ENCODE, and facilitates conversion rates up to 140 MSPS. Demuxed output mode is recommended for guaranteed operation above 100 MSPS, but may be enabled at any specified conversion rate.

Two data formats are possible in Dual Channel output mode, parallel data out and interleaved data out. Pin 75 I/P should be LOW for parallel format and HIGH for interleaved format. Figures 1 and 2 show the timing requirements for each format. Note that the Data Sync input, (DS), is required in Dual Channel output mode for both formats. The section on Data Sync describes the requirements of the Data Sync input.

As shown in Figures 1 and 2, when using the interleaved data format, a sample is taken on an ENCODE rising edge N. The resulting data is produced on an output port following the fifth rising edge of ENCODE after the sample was taken, (five pipeline delays). The following sample, (N+1), will be produced on the opposite port, also five pipeline delays after it was taken. The state of CLKOUT when the sample was taken will determine out of which port the data will come. If CLKOUT was LOW, the data will come out Port A. If CLKOUT was HIGH, the data will come out Port B.

In order to achieve parallel data format on the two output data ports, the data is internally aligned. This is accomplished by adding an extra pipeline delay to just the A Data Port. Thus, data coming out Port A will have six pipeline delays and data coming out Port B will have five pipeline delays. As with the interleaved format, the state of Data Sync when a sample is taken will determine out of which port the data will come. If CLKOUT was LOW, the data will come out Port A. If CLKOUT was HIGH, the data will come out Port B.

Data Sync

The Data Sync input, DS, is required to be driven for most applications to guarantee at which output port a given sample will appear. *When DS is held high, the ADC data outputs and clock outputs do not switch—they are held static.* Synchronization is accomplished by the assertion (falling edge) of DS, within the timing constraints T_{SDS} and T_{HDS} relative to an encode rising edge. (On initial synchronization T_{HDS} is not relevant.) If DS falls T_{SDS} before a given encode rising edge N, the analog value at that point in time will be digitized and available at Port A five cycles later (interleaved mode). The very next sample, N+l, will be sampled by the next rising encode edge and available at Port B five cycles after that encode edge (interleaved mode). In dual parallel mode the A port has a six cycle latency, the B port has a five cycle latency as described in Demuxed Outputs Mode section.

DS can be asserted once per video line if desired by using the horizontal sync signal (HSYNC). The start of HSYNC should occur after the end of active video by at least the chip latency. The HSYNC front porch is usually much greater than this in a typical SXGA system. If this is true in a given system then DS can be reset high by the HSYNC leading edge (the samples at that point should not be required in a typical system). DS can then be reasserted (brought low), by triggering from HSYNC trailing edge—observing T_{SDS} of the next rising encode edge. The first pixel data (on A Port) would be available five cycles after the first rising encode after HSYNC goes high.

It is possible to use the phase of the data clock outputs and software programming to accommodate situations where DS is not driven. The data clock outputs (CLKOUT and $\overline{\text{CLKOUT}}$) can be used to determine when data is valid on the output ports. In these cases DS should be grounded and $\overline{\text{DS}}$ left floating or connected to V_{CC}. If CLKOUT was low when a given sample was taken, the digitized value will be available on Port A, five cycles later. Data Sync has no effect when Single Channel Mode is selected, it should be grounded

Figure 2 shows how to use DS properly. The DS rising edge does not have any special timing requirements except that no data will come out of either port while it is held HIGH. The falling edge of DS must, however, meet a minimum setup-and-hold time with respect to the rising edge of ENCODE.

Single Channel Outputs Mode

In Single Channel mode, (Pin 74 OMS = HIGH), the timing of the AD9483 is similar to any high speed ADC (Figure 1). A sample is taken on every rising edge of ENCODE, and the resulting data is produced on the output pins following the fourth rising edge of ENCODE after the sample was taken, (four pipeline delays). The output data are valid t_{PD} after the rising edge of ENCODE, and remain valid until at least t_V after the next rising edge of ENCODE.

The maximum conversion rate in the mode should be limited to 100 MSPS. This is recommended because the guaranteed output data valid time minus the propagation delay is only 4 ns at 100 MSPS. This is about as fast as standard logic is able to capture the data with reasonable design margins. The AD9483 will operate faster in this mode if the user is able to capture the data.

When operating in single channel mode, all data comes out the A Ports while the B Ports are held static in a random state.

Data Clock Outputs

The data clock outputs will switch at two potential frequencies. In Single Channel mode, where all data comes out of Port A at the full ENCODE rate, the data clock outputs switch at the same frequency as the ENCODE. In Dual Channel mode, where the data alternates between the two ports, each of which operate at 1/2 the full ENCODE rate, the data clock outputs also switch at 1/2 the full ENCODE rate.

The data clock outputs have two potential purposes. The first is to act as a latch signal for capturing output data. In order to do this, simply drive the data latches with the appropriate data clock output. The second use is in Dual Channel data mode to help determine out of which data port data will come out. Refer to Figure 2 for a complete timing diagram, but in this mode, a rising edge on data clock will correspond to data switching on data Port B.

LAYOUT AND BYPASSING CONSIDERATIONS

Proper high speed layout and bypassing techniques should be used with the AD9483. Each V_{CC} and V_{DD} power pin should be bypassed as close to the pin as possible with a 0.01 µF to 0.1 µF capacitor Also, one 10 µF capacitor to ground should be used per supply per board. The VREF OUT pin and each of the three VREF IN pins should also be bypassed with a 0.01 µF to 0.1 µF capacitor to ground.

A single, substantial, low impedance ground plane should be place under and around the AD9483. Try to maximize the distance between the sensitive analog signals, (AIN, VREF), and the digital signals. Capacitive loading on the digital outputs should be kept to a minimum. This can be facilitated by keeping the traces short and in the case of the clock outputs by driving as few other devices as possible. Socketing the AD9483 should also be avoided. Try to match trace lengths of similar signals to avoid mismatches in propagation delays, (the encode inputs, analog inputs, digital outputs).

POWER SUPPLIES

At power up, V_{CC} must come up before V_{DD}. V_{CC} is considered the converter supply, nominally 5.0 V (±5.0%) V_{DD} is consider output power supply, nominally 3.3 V (±10%) or 5.0 V (±5%). At power off, V_{DD} must turn off first. Failure to observe the correct power supply sequencing many damage this device.

EVALUATION BOARD

The AD9483 evaluation board offers an easy way to test the AD9483. It provides ac or dc biasing for the analog input, it generates the output latch clocks for Single Mode, Dual Parallel Mode and Dual Interleaved Mode. Each of the three channels has a reconstruction DAC (A Port only). The board has several different modes of operation, and is shipped in the following configuration:

- Single-ended ac coupled analog input (1 V p-p centered at ground)
- Differential clock inputs (PECL) (See ENCODE section for TTL drive)
- Internal voltage references connected to externally buffered on-chip reference (VREF OUT)
- Preset for Dual Mode Interleaved

Analog Input

The evaluation board accepts a 1 V p-p input signal centered at ground for ac coupled input mode (Set Jumpers W4, W5, W12, W13, W18, W17 to jump Pin 1 to Pin 2). This signal biased up to 2.5 V by the on-chip reference. Note: input signal should be bandlimited (filtered) prior to sampling to avoid aliasing. The analog inputs are terminated to ground by a 75 Ω resistor on the board. The analog inputs are ac coupled through 0.1 µF caps C2, C4, C6 on top of the board. These can be increased to accommodate lower frequency inputs if desired using test points PR1–PR6 on bottom of board. In dc coupled input mode (Set Jumpers W4, W5, W12, W13, W18, W17 to jump Pin 3 to Pin 2) the board accepts typical video level signal levels (0 mV to 700 mV) the signal is level shifted and amplified to 1 V p-p by the AD8055 preamp. Trimpots R98–R100 are used to adjust dc black level to 2 V at ADC inputs.

Encode

The AD9483 ENCODE input can be driven two ways.

1. Differential PECL (V_{LO} = 3, V_{HI} = 4 nominal). It is shipped in this mode.
2. Single ended TTL or CMOS. (At Encode Bar–Remove 50 Ω termination resistor R10, add 0.1 µF capacitor C7)

Voltage Reference

The AD9483 has an internal 2.5 V voltage reference (VREF OUT). This is buffered externally on board to support additional level shifting circuitry (the AD9483 VREF OUT pin can drive the three VREF IN pins in applications where level shifting is not required with no additional buffering). An external reference may be employed instead to drive each VREF IN pin independently (requires moving Jumpers W14, W15 and W16).

Single Channel Mode

Single Channel mode sets the AD9483 to produce data on every clock cycle on output port A only. The maximum speed in Single Channel mode is 100 MSPS.

Dual Channel Modes (Outputs Clocked at 1/2 Encode Clock)

Dual Channel Interleaved

Sets the ADC to produce data alternately on Port A and Port B. the maximum speed in this mode is 140 MSPS.

Dual Channel Parallel

Sets the ADC to produce data concurrently on Port A and Port B. Maximum speed in this mode is 140 MSPS.

DAC Out

The DAC output is a representation of the data on output Port A only. The DAC is terminated on the board into 75 Ω. Full-scale voltage swing at DAC output is nominally 0 mV to 800 mV when terminated into external 75 Ω (doubly terminated).

Output Port B is *not* reconstructed. The DAC outputs are NOT filtered and will exhibit sampling noise. The DACs can be powered down at W1, W2, and W3 (jumper not installed).

Data Ready

An output clock for latching the ADC outputs is available at Pin 1 at the 25-pin connector. Its complement is located at Pin 14. The clocks are terminated on the board by a 75 Ω Thevenin termination to $V_D/2$. The timing on these clock outputs can be inverted at W9, W10 (jumper not installed).

Schematics

The schematics for the evaluation board follow. (Note bypass capacitors for ADC are shown in Figure 39.)

Table III. Evaluation Board Jumper Settings

MODE	W7 (OMS)	W6 (I/P)	W11 (A_LAT)	W11 (B_LAT)
Dual Channel/PARALLEL	LOW	LOW	$\overline{\text{DATA_CLK_OUT}}$ (4–5)	$\overline{\text{DATA_CLK_OUT}}$ (2–3)
Dual Channel/INTERLEAVED	LOW	HIGH	DATA_CLK_OUT (5–6)	DATA_CLK_OUT (2–3)
SINGLE	HIGH	DON'T CARE	DATA_CLK_OUT (5–6)	NC

DESIGN NOTES
Maximum frequency for PARALLEL is 140 MHz.
Maximum frequency for INTERLEAVED is 140 MHz.
Maximum frequency for SINGLE is 100 MHz.
DS is tied to ground through a 50 Ω resistor.
$\overline{\text{DS}}$ is left floating.

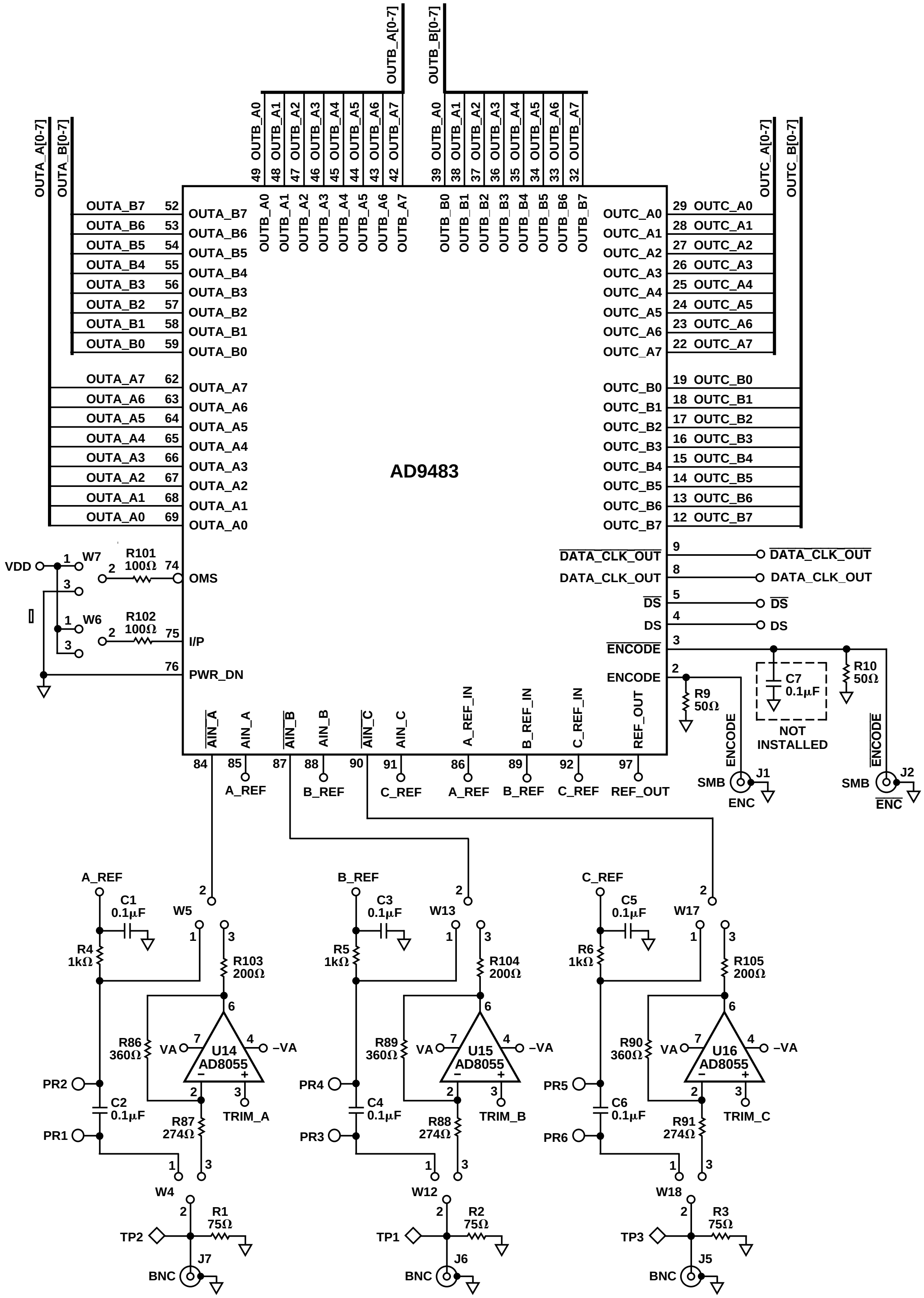


Figure 35. ADC and Preamp Section

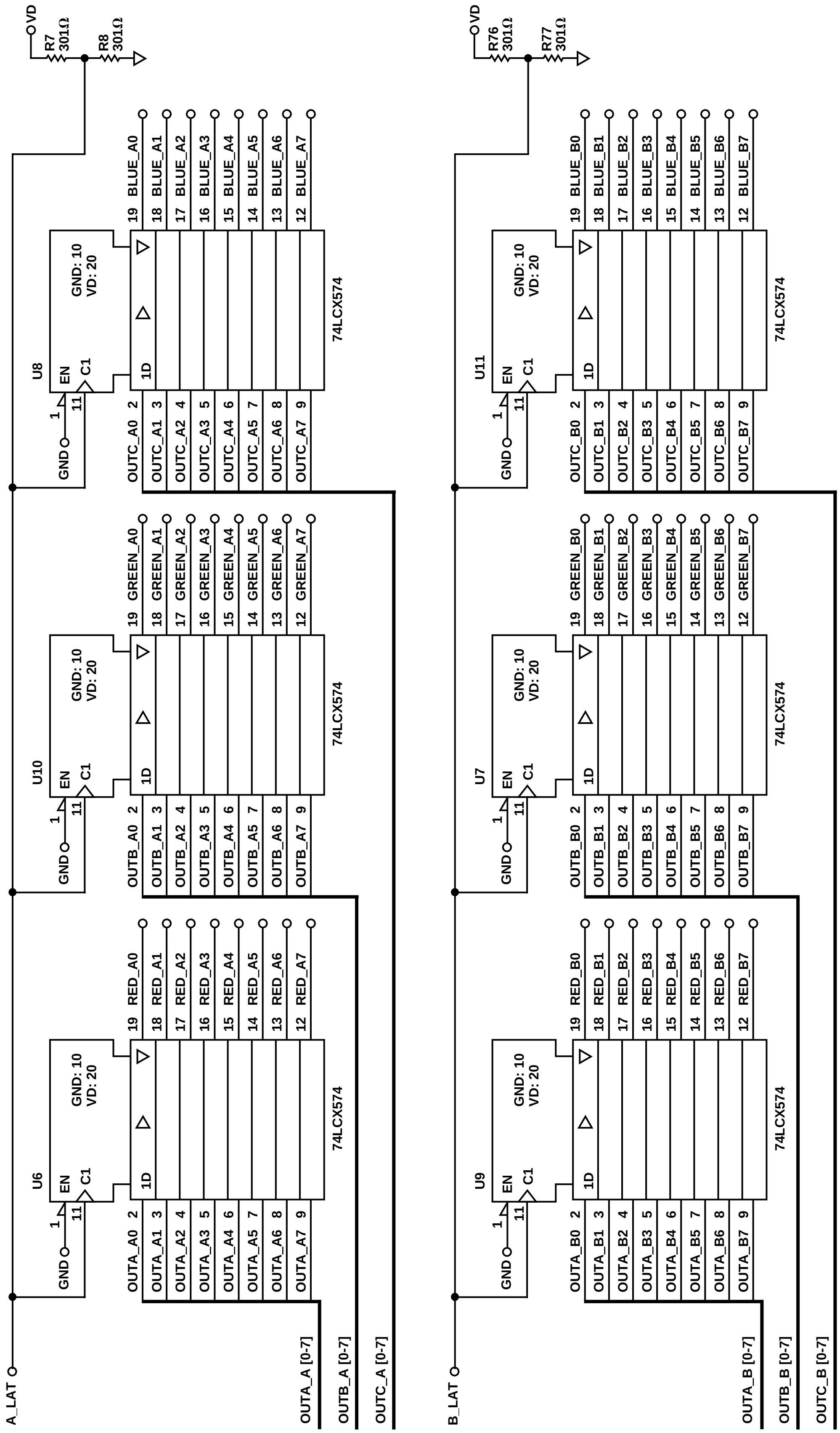


Figure 36. Output Latches Section

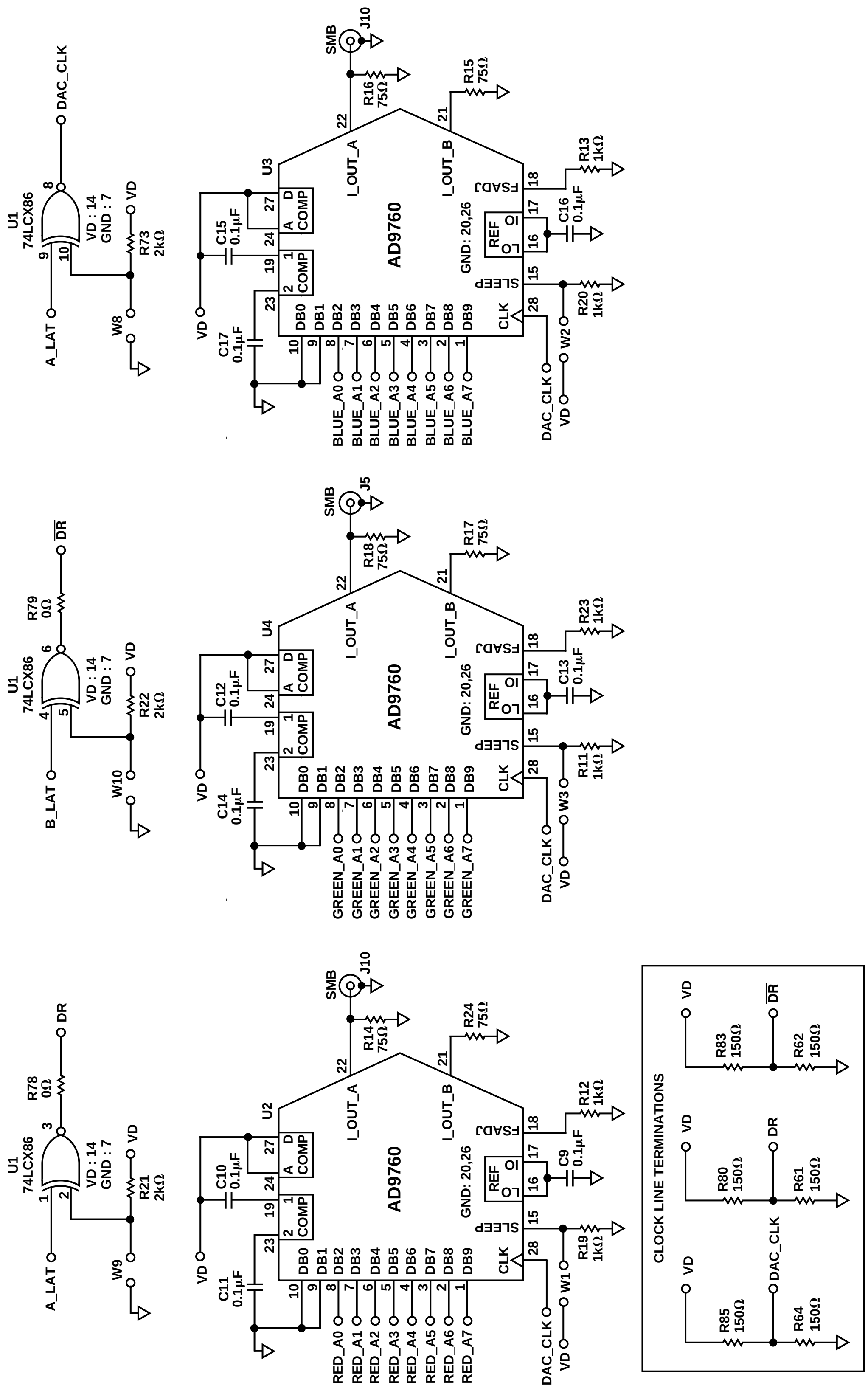


Figure 37. DACs and Clock Buffer Section

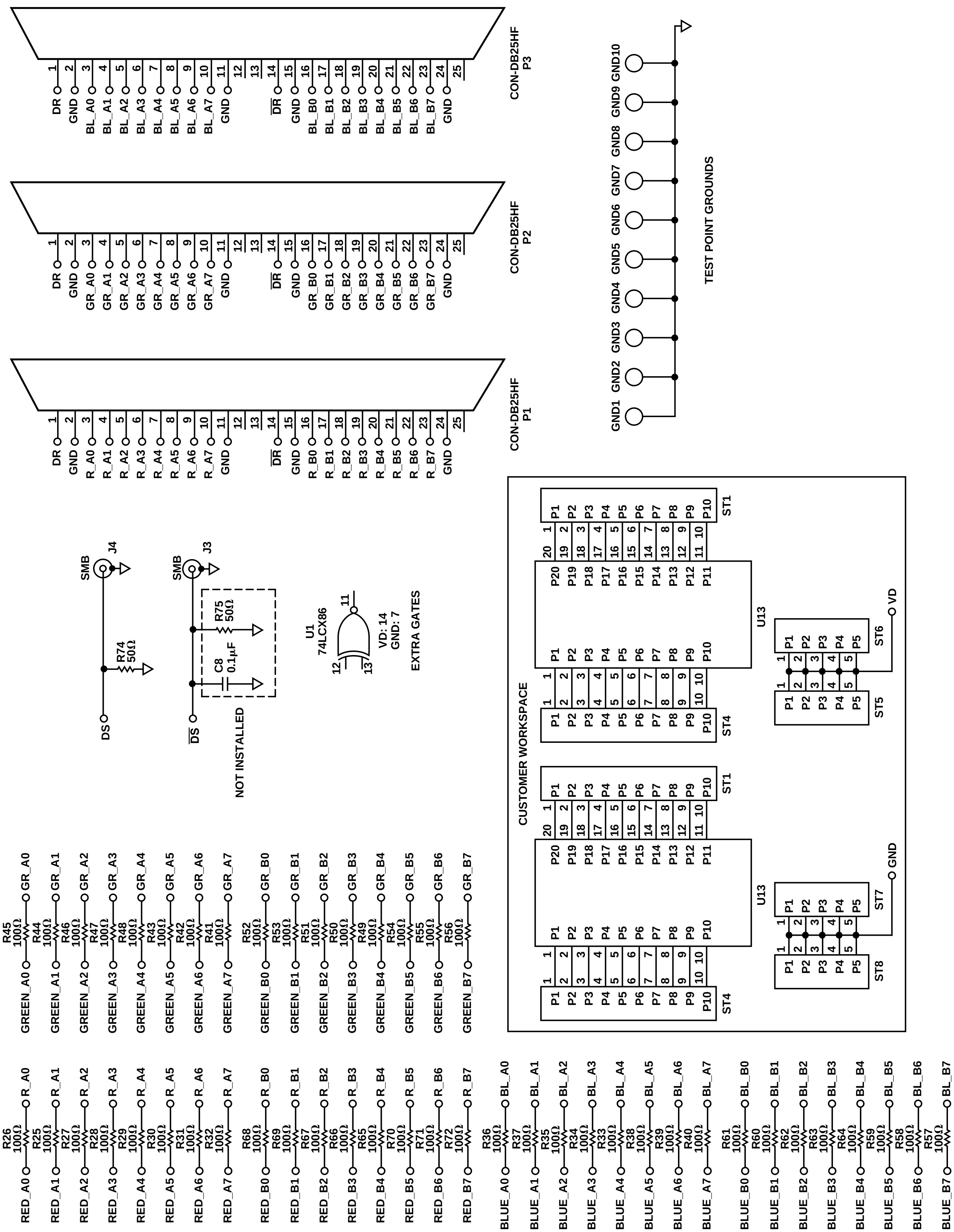


Figure 38. Digital Outputs Connectors and Terminations Section

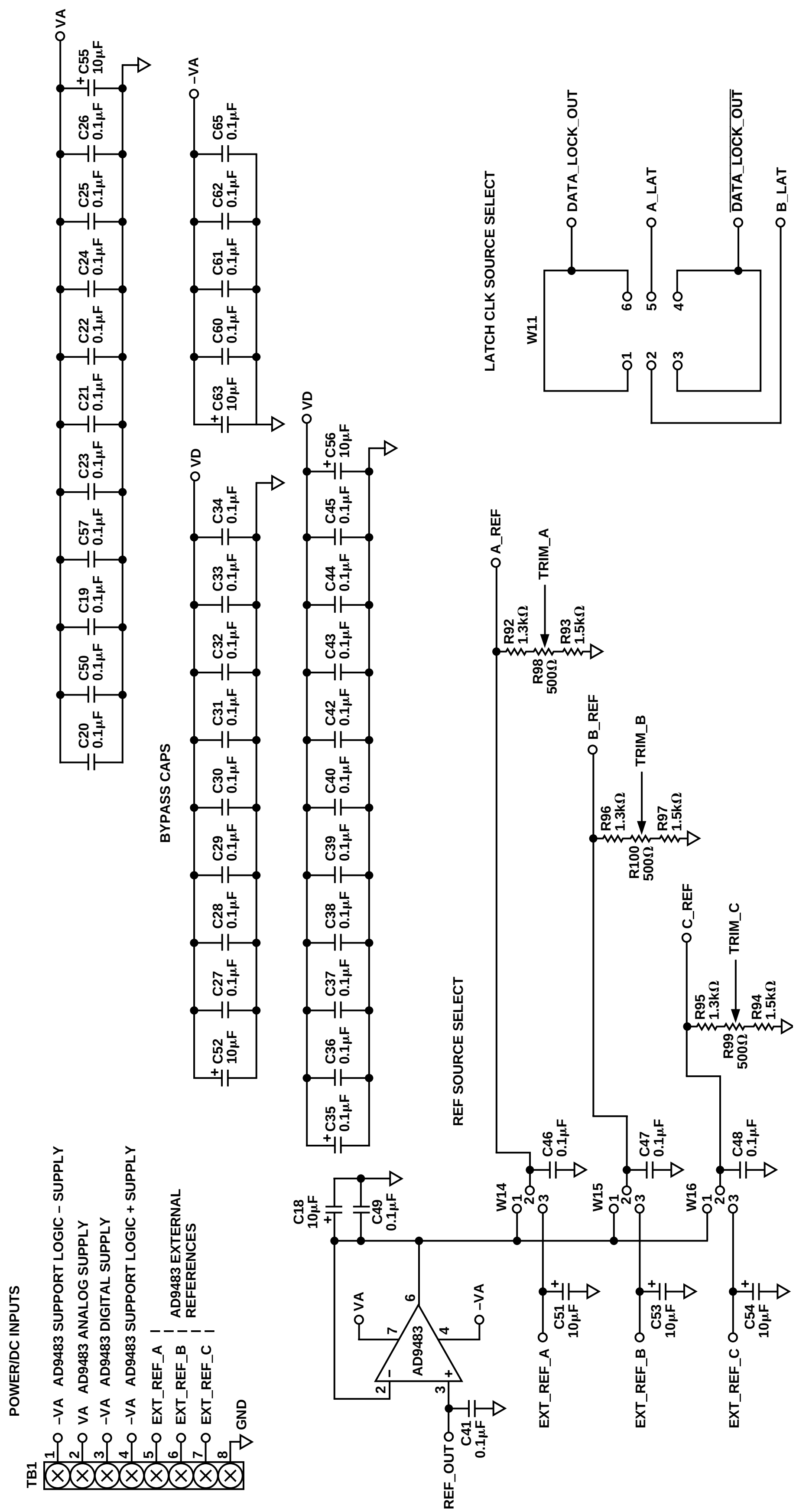


Figure 39. Power Connector, Decoupling Capacitors, DC Adjust Trimpot Section

PCB LAYOUT

The PCB is designed on a four layer (1 oz. Cu) board. Components and routing are on the top layer with a ground flood for additional isolation. Test and ground points were judiciously placed to facilitate high speed probing. Each channel has a separate 25-pin connector for it's digital outputs. A common ground plane exists on the second layer.

The third layer has the 3 split power planes:

1. 5 V analog for the ADC and preamps,
2. 3.3 V (or 5 V) ADC output supply, and
3. A separate 3.3 V supply for support logic. The fourth layer contains the –5 V plane for the preamps and additional components and routing. There is additional space for two extra components on top of the board to allow for modification.

Table IV. 25-Pin Connector Pinout

Pin No.	Pin Name
1	DR (Data Ready)
2	GND
3	A0
4	A1
5	A2
6	A3
7	A4
8	A5
9	A6
10	A7
11	GND
12	NC (No Connect)
13	NC (No Connect)
14	DRB (Data Ready Bar)
15	GND
16	B0
17	B1
18	B2
19	B3
20	B4
21	B5
22	B6
23	B7
24	GND
25	NC (No Connect)

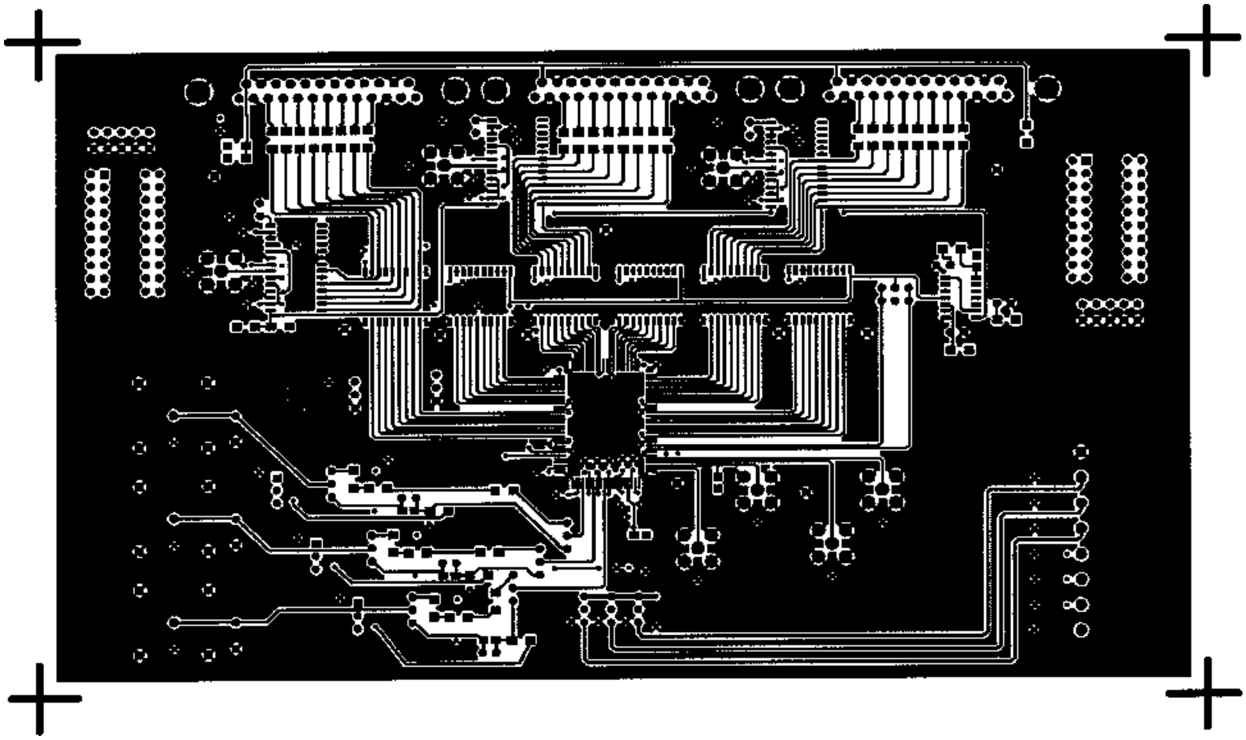


Figure 40. Layer 1. Routing and Top Layer Ground

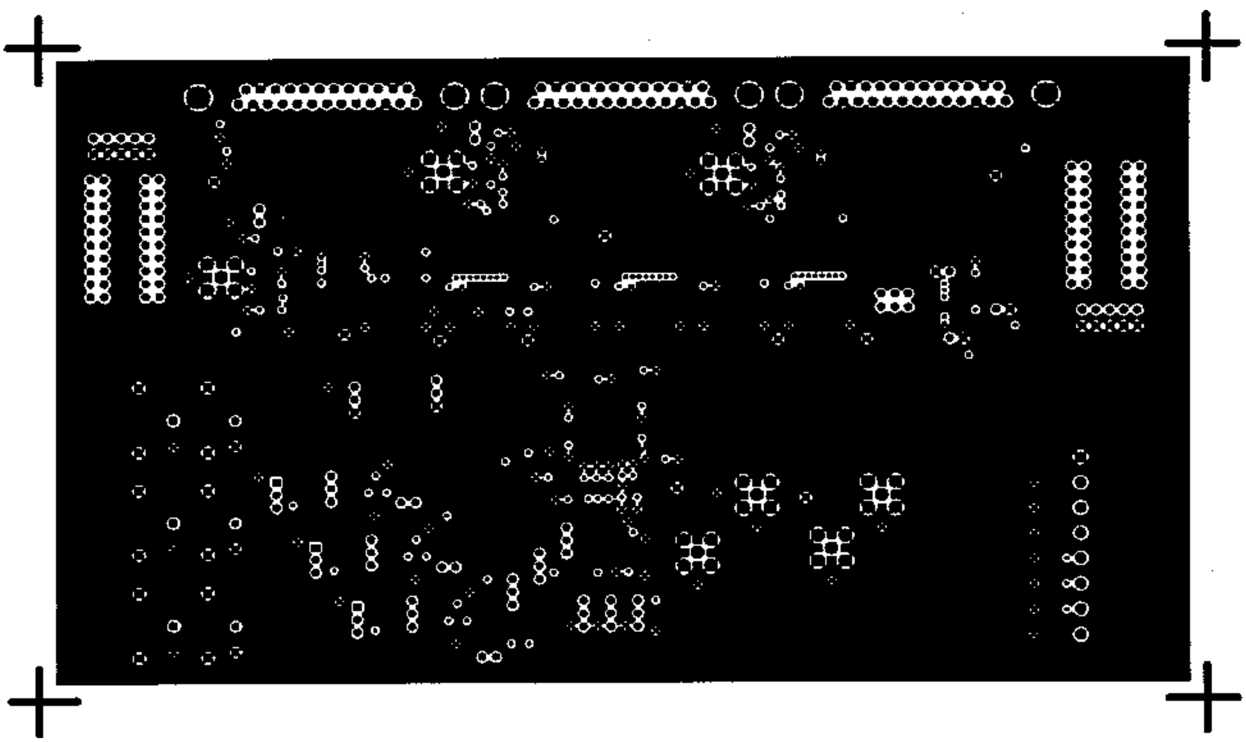


Figure 41. Layer 2 Ground Plane

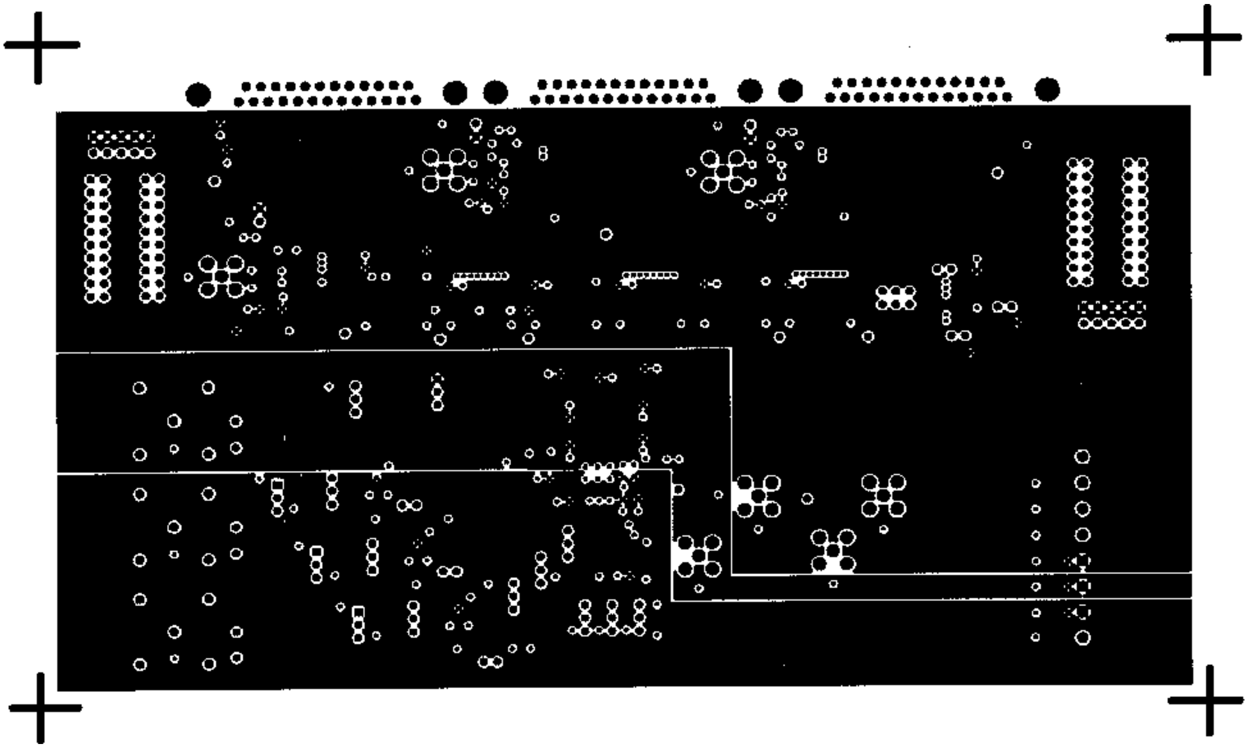


Figure 42. Layer 3 Split Power Planes

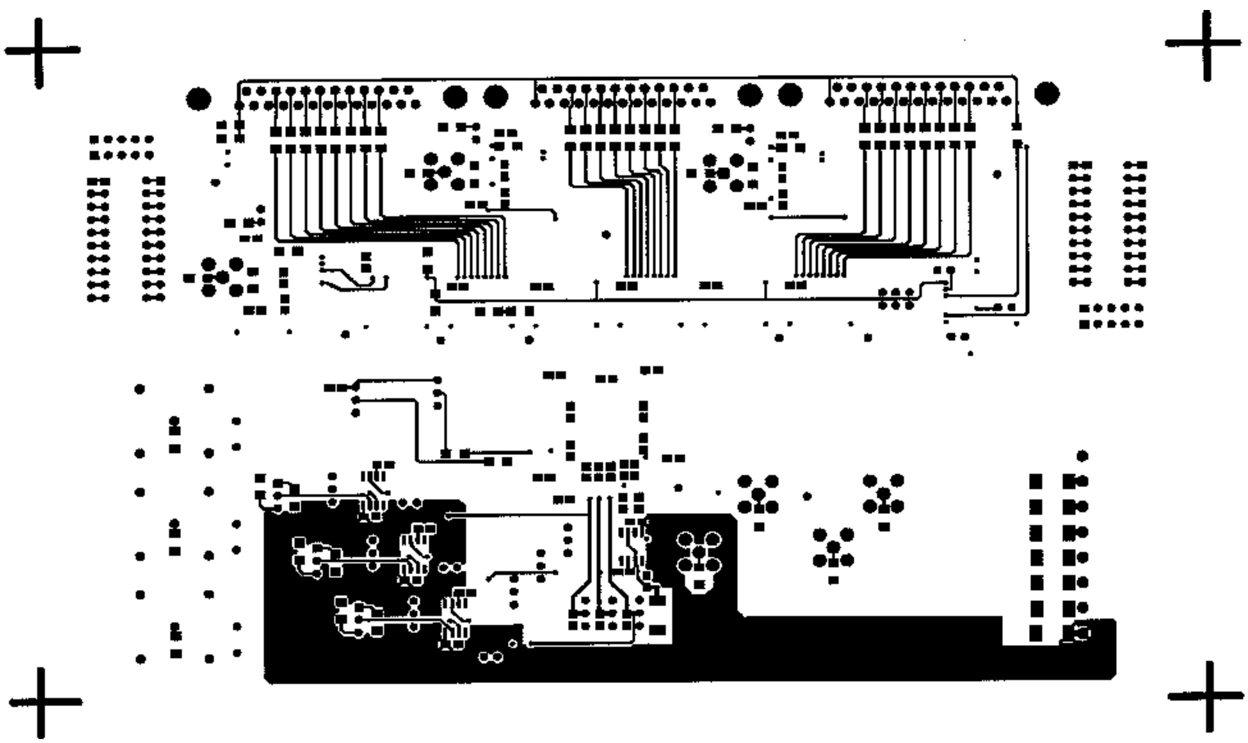


Figure 43. Layer 4 Routing and Negative 5 V

EVALUATION BOARD PARTS LIST

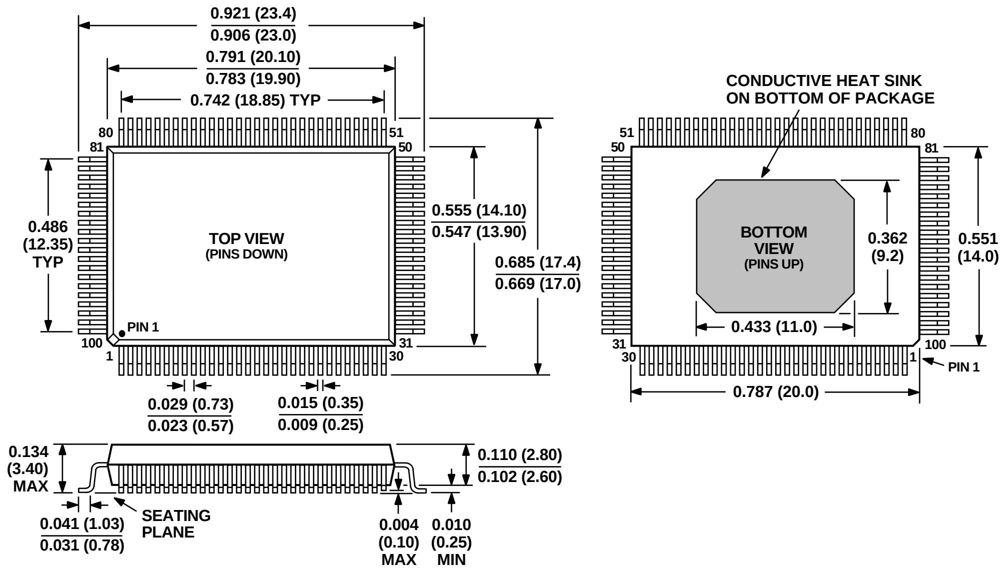
#	QTY	REFDES	DEVICE	PACKAGE	PART NUMBER	VALUE	SUPPLIER
1	54	C1-17, C19-50, C57, C60-62, C65	CAPACITOR	0805	C0805C104K5RAC7025	0.1 µF	KEMIT
2	8	C18, C51-56, C63	CAPACITOR	TAJD	T491C106K016AS	10 µF	KEMIT
3	16	GND1-10, PR1, PR2, PR3, PR4, PR5, PR6	PART OF PCB	OMIT			
4	7	J1-4, J8-10	CONNECTOR	SMB	B51-351-000-220		ITT CANNON
5	3	J5-7	CONNECTOR	BNC	227699-2		AMP
6	3	P1-3	CONNECTOR	"D" 25 PINS	745783-2		AMP
7 8	9 9	R1-3, R14-18, R24 R4-6, R11-13, R19-20, R23	RESISTOR RESISTOR	1206 1206	CRCW120675R0FT CRCW12061001FT	75 Ω 1K	DALE DALE
9	4	R7-8, R76-77	RESISTOR	1206	CRCW12063010FT	301 Ω	DALE
10	4	R9-10, R74-75	RESISTOR	1206	CRCW120649R9FT	49.9 Ω	DALE
11	3	R21-22, R73	RESISTOR	1206	CRCW12062001FT	2K	DALE
12	50	R25-72, R101-102	RESISTOR	1206	CRCW12061000FT	100 Ω	DALE
13	2	R78-79	RESISTOR	1206	CRCW1206000ZT	0 Ω	DALE
14	6	R80-85	RESISTOR	1206	CRCW12061500FT	150 Ω	DALE
15	3	R86, R89-90	RESISTOR	1206	CRCW12063600FT	360 Ω	DALE
16	3	R87-88, R91	RESISTOR	1206	CRCW12062740FT	274 Ω	DALE
17	3	R92, R95-96	RESISTOR	1206	CRCW12061301FT	1.3K	DALE
18	3	R93-94, R97	RESISTOR	1206	CRCW12061501FT	1.5K	DALE
19	3	R98-100	TRIMMER	VRES	3296W001501	500 Ω	BOURNES
20	2	R103-105	RESISTOR	1206	CRCW12062000F	200 Ω	DALE
21	4	ST1-4	PART OF PCB	STRIP10	NOT INSTALLED		
22	4	ST5-8	PART OF PCB	STRIP5	NOT INSTALLED		
23	1	TB1	POWER CONNECTOR (2 PIECE)	TB8A	95F6002 50F3583		WIELAND
24	3	TP1-3	PART OF PCB	TSTPT	NOT INSTALLED		
25	1	U1	MC74LCX86D	SO14NB	MC74LCX86D		MOTOROLA
26	3	U2-4	AD9760AR	SO28WB	AD9760AR		ADI
27	1	U5	AD9483KS-140/100	MQFP-100	AD9483KS-140/100		ADI
28	6	U6-11	MC74LCX574DW	SO20WB	MC74LCX574DW		MOTOROLA
29	4	U12, U14-16	AD8055AN	SO8NB	AD8055AN		ADI
30	2	U13, U17	DIP20	DIP20	NOT INSTALLED		
31	6	W1-3, W8-10	2 PIN JUMPER	JMP-2P	SEE NOTE		
32	11	W4-7, W12-18	3 PIN JUMPER	JMP-3P	SEE NOTE		
33	1	W11	6 PIN JUMPER	JMP_6	SEE NOTE		
34	5	FEET	SJ-5518				3M

NOTES
All resistors are surface mount (size 1206) and have a 1% tolerance.
Jumpers are Samtec parts TSW-110-08-G-D and TSW-110-08-G-S.
Jumpers W1, W2, W3, W9, W8, W10 are omitted.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

100-Lead Plastic Quad Flatpack (S-100B)



NOTE: THE AD9483KS PACKAGE USES A COPPER INSERT TO HELP DISSIPATE HEAT AND ENSURE RELIABLE OPERATION OVER THE FULL 0°C TO +85°C TEMPERATURE RANGE. THIS COPPER INSERT IS EXPOSED ON THE UNDERSIDE OF THE DEVICE. IT IS RECOMMENDED THAT DURING THE DESIGN OF THE PC BOARD NO THROUGHHOLES OR SIGNAL TRACES BE PLACED UNDER THE AD9483 THAT COULD COME IN CONTACT WITH THE COPPER INSERT. COMMONLY ACCEPTED BOARD LAYOUT PRACTICES FOR HIGH SPEED CONVERTERS SPECIFY THAT ONLY GROUND PLANES SHALL BE LOCATED UNDER THESE DEVICES TO MINIMIZE NOISE OR DISTORTION OF VIDEO SIGNALS.

C3268a–1–12/98

PRINTED IN U.S.A.